Reg.No. \_\_\_\_\_\_\_\_\_\_\_\_



**End Semester Examination – Nov/Dec – 2018**

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| **Code :** | **18EC3027** | **Duration :** | **3hrs** |
| **Sub. Name :** | **CMOS VLSI DESIGN** | **Max. marks :** | **100** |

**ANSWER ANY FIVE QUESTIONS (5 x 16 = 80 Marks)**

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| **Q. No.** | **Sub Div.** | **Questions** | **Course**  **Outcome** | **Marks** |
| 1. | a. | Derive the expression for threshold voltage of a MOS transistor and explain the significance of different parameters present in the equation. | CO1 | 8 |
| b. | Discuss the principles of constant field scaling and lateral scaling. Write the effects of above scaling methods on the device characteristics. | CO1 | 8 |
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| 2. | a. | Draw and explain CMOS DC transfer characteristics and mark all the regions of operations with necessary equations. | CO2 | 12 |
| b. | Compare CMOS and Bipolar technology. | CO2 | 4 |
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| 3. | a. | Mention the basic principles in design of dynamic CMOS and discuss in brief about it with neat sketch. | CO3 | 12 |
| b. | Draw the gate level and transistor level schematic diagram of Full adder circuit. | CO3 | 4 |
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| 4. |  | Write the short notes on .   1. True Single Phase Clocked Register. 2. NORA- CMOS Latch. | CO4 | 8+8 |
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| 5. |  | Design and explain in detail about the logic consideration of binary adder with neat example. | CO5 | 16 |
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| 6. | a. | Briefly discuss about the noise margin involve in CMOS inverter with neat diagram. | CO2 | 8 |
| b. | Explain the switching characteristics of CMOS inverter and analysis the different types of delays. | CO2 | 8 |
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| 7. |  | Discuss about the design of sequential logic circuit design and its pipelining concept to optimize the sequential circuit. | CO5 | 16 |
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| **COMPULSORY QUESTION (1 x 20 = 20 Marks)** | | | | |
| 8. |  | Explain the concept of carry save multiplier and barrel shifter with its neat architecture also mention power and speed trade off in data path circuits. | CO6 | 20 |